

NTMFD4C85N

PowerPhase, Dual N-Channel SO8FL 30 V, High Side 25 A / Low Side 49 A

Features

- Co-Packaged Power Stage Solution to Minimize Board Space
- Minimized Parasitic Inductances
- Optimized Devices to Reduce Power Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- DC-DC Converters
- System Voltage Rails
- Point of Load

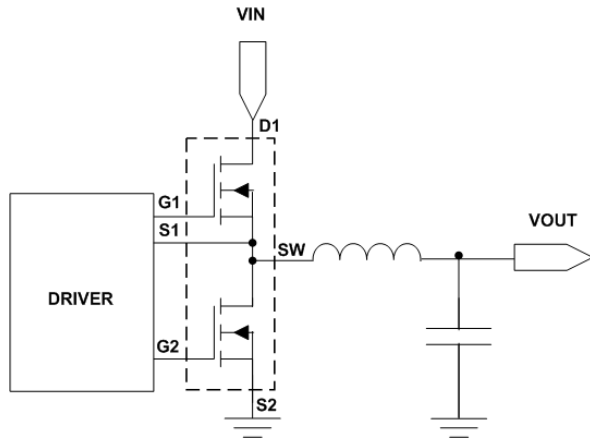


Figure 1. Typical Application Circuit

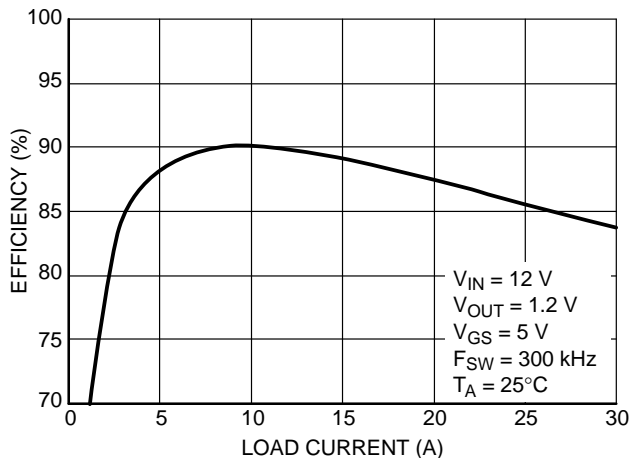


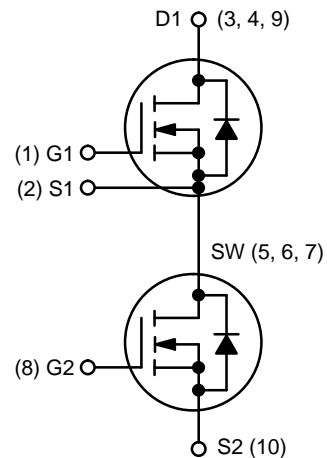
Figure 2. Typical Efficiency Performance
POWERPHASEGEVB Evaluation Board



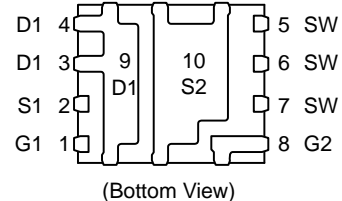
ON Semiconductor®

www.onsemi.com

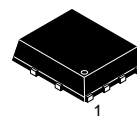
V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
Q1 Top FET 30 V	3.0 mΩ @ 10 V	25 A
	4.3 mΩ @ 4.5 V	
Q2 Bottom FET 30 V	0.8 mΩ @ 10 V	49 A
	1.2 mΩ @ 4.5 V	



PIN CONNECTIONS



MARKING DIAGRAM



DFN8
CASE 506CR



- 4C85N = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

NTMFD4C85N

Table 1. MAXIMUM RATINGS (T_J=25°C unless otherwise stated)

Parameter			Symbol	Value	Units
Drain-to-Source Voltage	Q1	V _{DSS}	30	V	
	Q2				
Gate-to-Source Voltage	Q1	V _{GS}	±20	V	
	Q2				
Continuous Drain Current R _{θJA} (Note 1)	T _A = 25°C	Q1	I _D	20.1	A
				14.5	
	T _A = 85°C	Q2	39		
			28.1		
Power Dissipation R _{θJA} (Note 1)	T _A = 25°C	Q1	P _D	1.95	W
Continuous Drain Current R _{θJA} ≤ 10 s (Note 1)	T _A = 25°C	Q1	I _D	25.4	A
				18.3	
	T _A = 85°C	Q2	49.2		
			35.5		
Power Dissipation R _{θJA} ≤ 10 s (Note 1)	T _A = 25°C	Q1	P _D	3.10	W
Continuous Drain Current R _{θJA} (Note 2)	T _A = 25°C	Q1	I _D	15.4	A
				11.1	
	T _A = 85°C	Q2	29.7		
			21.4		
Power Dissipation R _{θJA} (Note 2)	T _A = 25°C	Q1	P _D	1.13	W
Pulsed Drain Current	T _A = 25°C t _p = 10 μs	Q1	I _{DM}	300	A
		Q2		525	
Operating Junction and Storage Temperature	Q1	T _J , T _{STG}	-55 to +150	°C	
	Q2				
Source Current (Body Diode)	Q1	I _S	10	A	
	Q2		10		
Drain to Source DV/DT		dV/dt	6	V/ns	
Single Pulse Drain-to-Source Avalanche Energy (T _J = 25°C, V _{DD} = 50 V, V _{GS} = 10 V, L = 0.1 mH, R _G = 25 Ω)	I _L = 19 A _{pk}	Q1	EAS	34.5	mJ
	I _L = 26 A _{pk}	Q2	EAS	222	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T _L	260	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 sq-in pad, 2 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size of 100 mm².

Table 2. THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Junction-to-Ambient – Steady State (Note 3)	R _{θJA}	64.2	°C/W
Junction-to-Ambient – Steady State (Note 4)		110.5	
Junction-to-Ambient – (t ≤ 10 s) (Note 3)		40.3	

3. Surface-mounted on FR4 board using 1 sq-in pad, 2 oz Cu
4. Surface-mounted on FR4 board using the minimum recommended pad size of 100 mm²

NTMFD4C85N

Table 3. ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	FET	Test Condition	Min	Typ	Max	Units		
OFF CHARACTERISTICS									
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	Q1	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V		
		Q2		30					
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS} / T_J$	Q1			19		mV/ $^\circ\text{C}$		
		Q2			17				
Zero Gate Voltage Drain Current	I_{DSS}	Q1	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1	μA		
				$T_J = 125^\circ\text{C}$		10			
		Q2		$T_J = 25^\circ\text{C}$		1			
Gate-to-Source Leakage Current	I_{GSS}	Q1	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA		
		Q2				100			
ON CHARACTERISTICS (Note 5)									
Gate Threshold Voltage	$V_{GS(TH)}$	Q1	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.3		2.1	V		
		Q2		1.3		2.1			
Negative Threshold Temperature Coefficient	$V_{GS(TH)} / T_J$	Q1			4.3		mV/ $^\circ\text{C}$		
		Q2			4.6				
Drain-to-Source On Resistance	$R_{DS(on)}$	Q1	$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}$		2.2	3.0	m Ω	
			$V_{GS} = 4.5\text{ V}$	$I_D = 20\text{ A}$		3.3	4.3		
		Q2	$V_{GS} = 10\text{ V}$	$I_D = 30\text{ A}$		0.6	0.8		
			$V_{GS} = 4.5\text{ V}$	$I_D = 30\text{ A}$		0.95	1.2		
CAPACITANCES									
Input Capacitance	C_{ISS}	Q1	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 15\text{ V}$		1960		pF		
		Q2			6660				
Output Capacitance	C_{OSS}	Q1			1230				
		Q2			3660				
Reverse Capacitance	C_{RSS}	Q1			102				
		Q2			126				
CHARGES & GATE RESISTANCE									
Total Gate Charge	$Q_{G(TOT)}$	Q1	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 20\text{ A}$		15		nC		
		Q2			45.2				
Threshold Gate Charge	$Q_{G(TH)}$	Q1			1.5				
		Q2			4.5				
Gate-to-Source Charge	Q_{GS}	Q1			5.0				
		Q2			15				
Gate-to-Drain Charge	Q_{GD}	Q1			5.2				
		Q2			11.8				
Total Gate Charge	$Q_{G(TOT)}$	Q1		$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}; I_D = 20\text{ A}$		32			nC
		Q2				99.3			
Gate Resistance	R_G	Q1	$T_A = 25^\circ\text{C}$		1.0		Ω		
		Q2			1.0				

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

6. Switching characteristics are independent of operating junction temperatures

NTMFD4C85N

Table 3. ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	FET	Test Condition	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 6)							
Turn-On Delay Time	$t_{d(ON)}$	Q1	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 20\text{ A}, R_G = 3.0\ \Omega$		10.3		ns
		Q2			19.5		
Rise Time	t_r	Q1			37		
		Q2			27		
Turn-Off Delay Time	$t_{d(OFF)}$	Q1			20		
		Q2			47		
Fall Time	t_f	Q1			5.6		
		Q2			15		

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	Q1	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 20\text{ A}, R_G = 3.0\ \Omega$		8.0		ns
		Q2			12.6		
Rise Time	t_r	Q1			31.5		
		Q2			22.7		
Turn-Off Delay Time	$t_{d(OFF)}$	Q1			25		
		Q2			60		
Fall Time	t_f	Q1			4.0		
		Q2			12.2		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Voltage	V_{SD}	Q1	$V_{GS} = 0\text{ V},$ $I_S = 10\text{ A}$	$T_J = 25^\circ\text{C}$		0.78	V
				$T_J = 125^\circ\text{C}$		0.62	
		Q2		$T_J = 25^\circ\text{C}$		0.75	
				$T_J = 125^\circ\text{C}$		0.55	

DRAIN-SOURCE DIODE CHARACTERISTICS

Reverse Recovery Time	t_{RR}	Q1	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 2\text{ A}$		40		ns	
		Q2			73			
Charge Time	t_a	Q1			20			
		Q2			40			
Discharge Time	t_b	Q1			20			
		Q2			33			
Reverse Recovery Charge	Q_{RR}	Q1			37			nC
		Q2			137			

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

6. Switching characteristics are independent of operating junction temperatures

NTMFD4C85N

TYPICAL CHARACTERISTICS – Q1

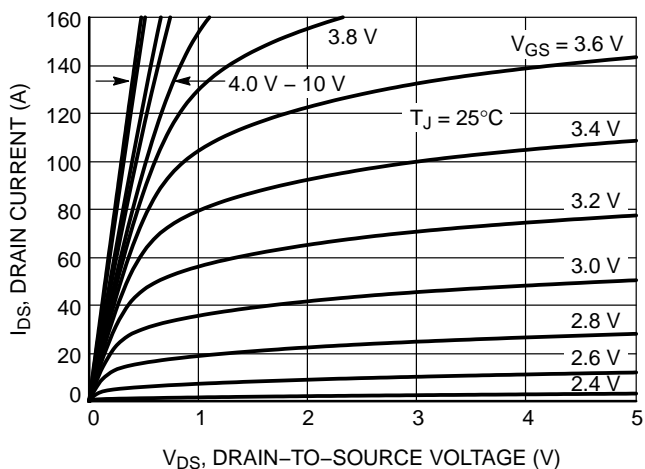


Figure 3. On-Region Characteristics

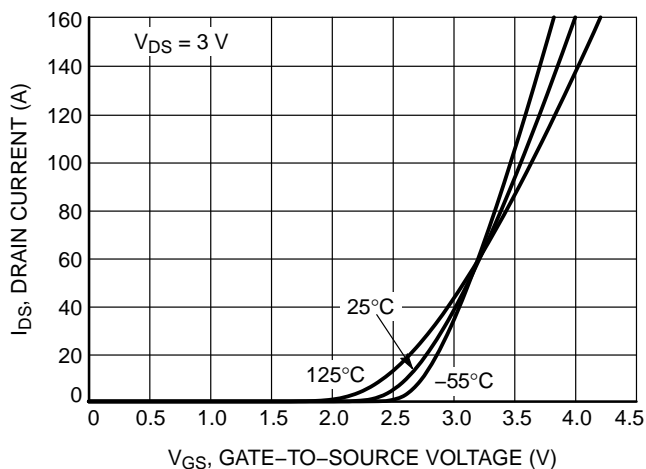


Figure 4. Transfer Characteristics

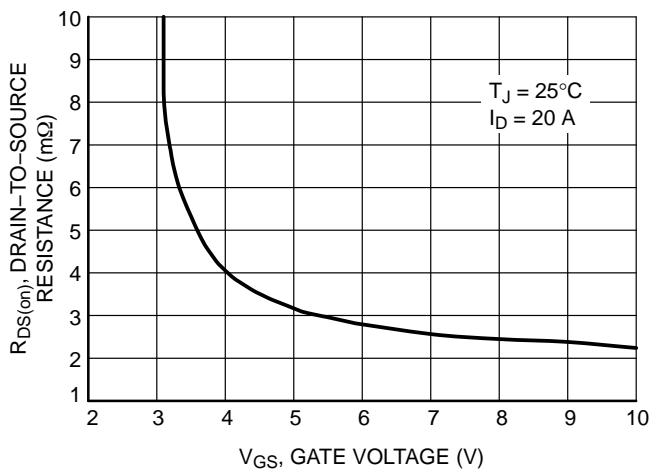


Figure 5. On-Resistance vs. Gate-to-Source Voltage

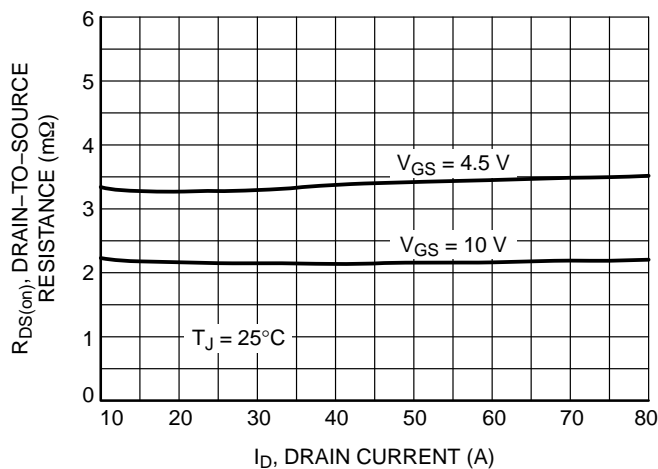


Figure 6. On-Resistance vs. Drain Current and Gate Voltage

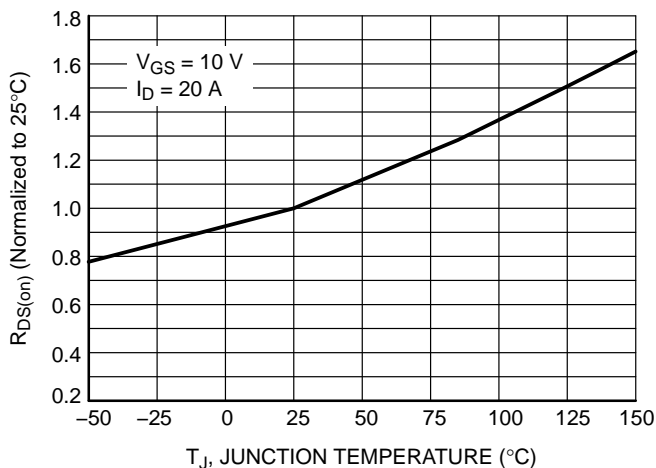


Figure 7. On-Resistance Variation with Temperature

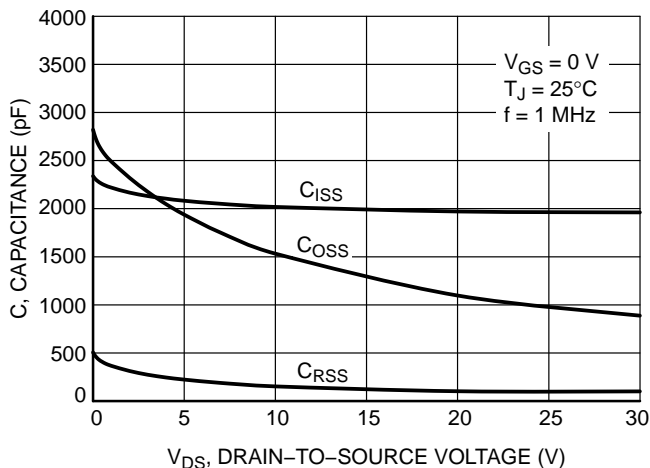


Figure 8. Capacitance Variation

NTMFD4C85N

TYPICAL CHARACTERISTICS – Q1

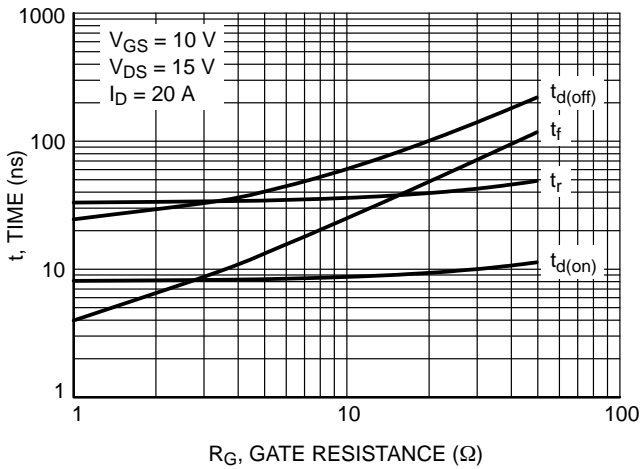


Figure 9. On-Region Characteristics

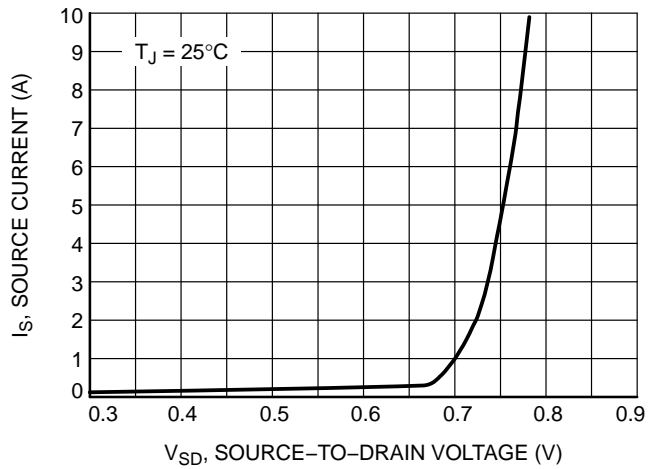


Figure 10. Diode Forward Voltage vs. Current

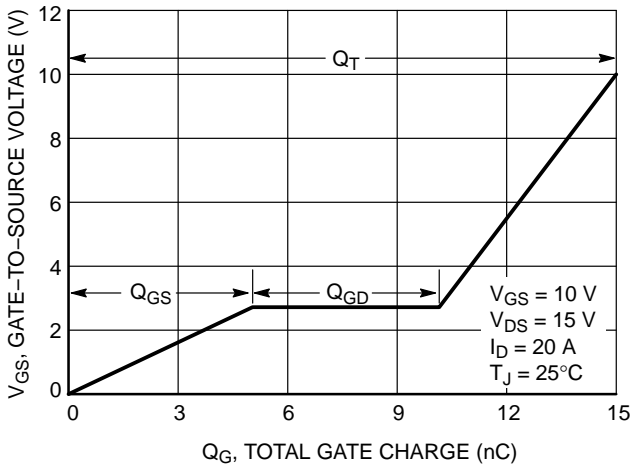


Figure 11. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

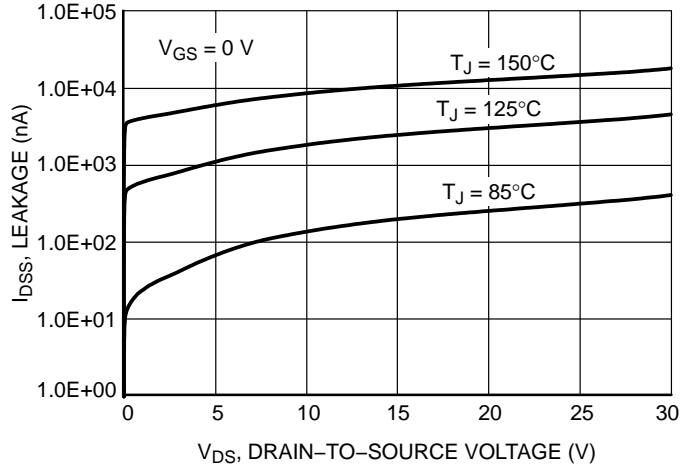


Figure 12. Drain-to-Source Leakage Current vs. Voltage

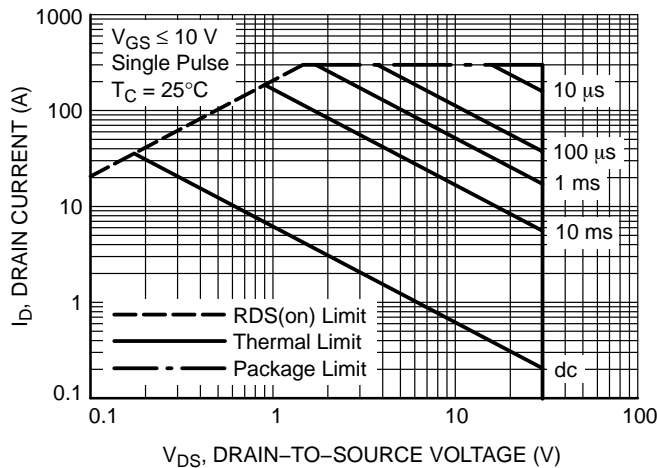


Figure 13. Maximum Rated Forward Biased Safe Operating Area

NTMFD4C85N

TYPICAL CHARACTERISTICS – Q1

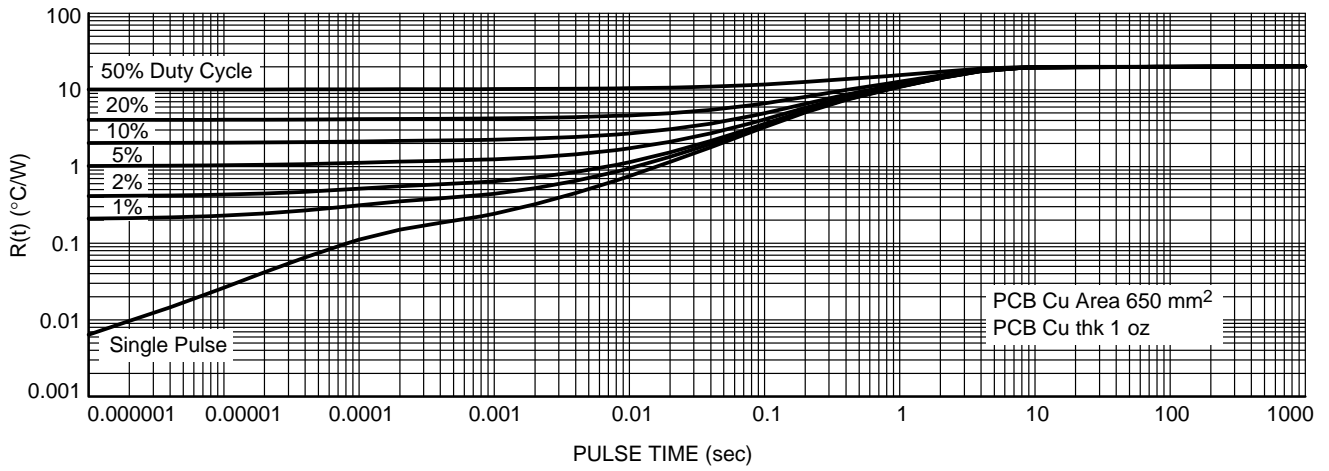


Figure 14. Thermal Characteristics

NTMFD4C85N

TYPICAL CHARACTERISTICS – Q2

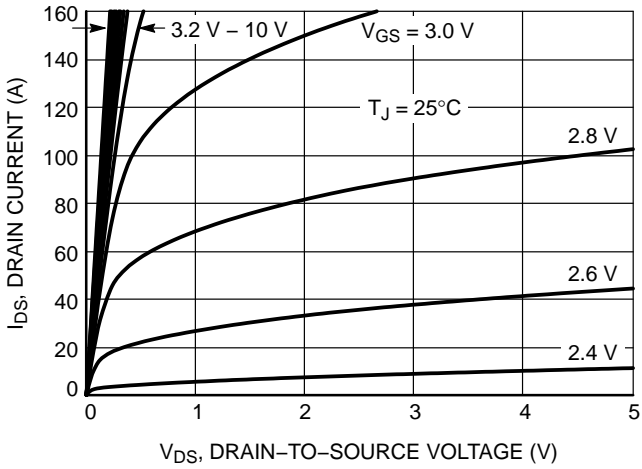


Figure 15. On-Region Characteristics

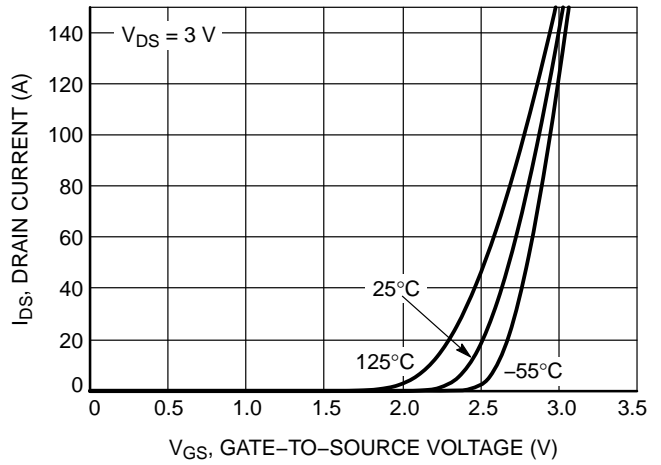


Figure 16. Transfer Characteristics

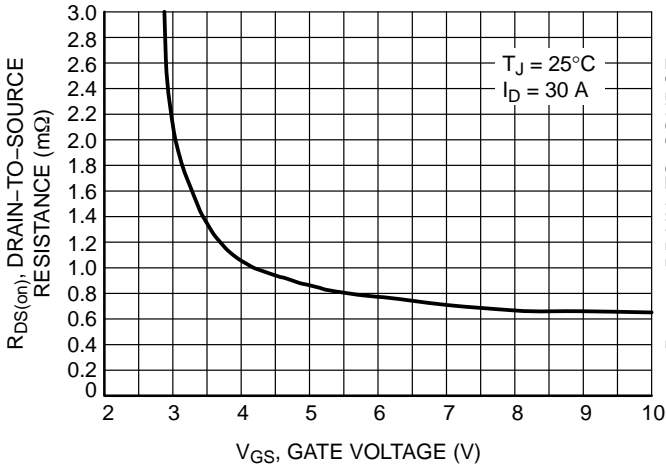


Figure 17. On-Resistance vs. Gate-to-Source Voltage

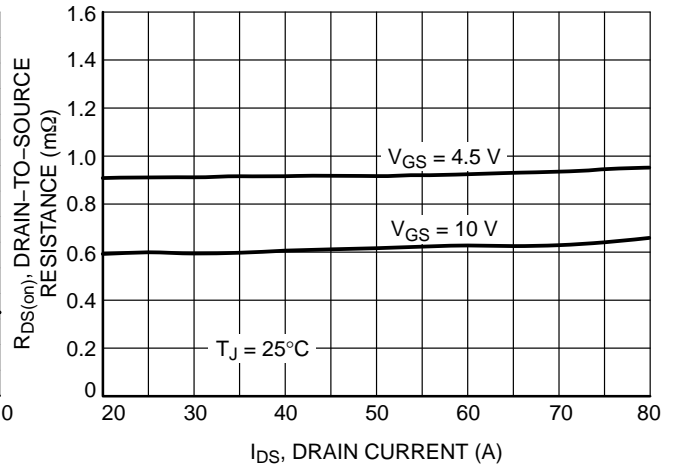


Figure 18. On-Resistance vs. Drain Current and Gate Voltage

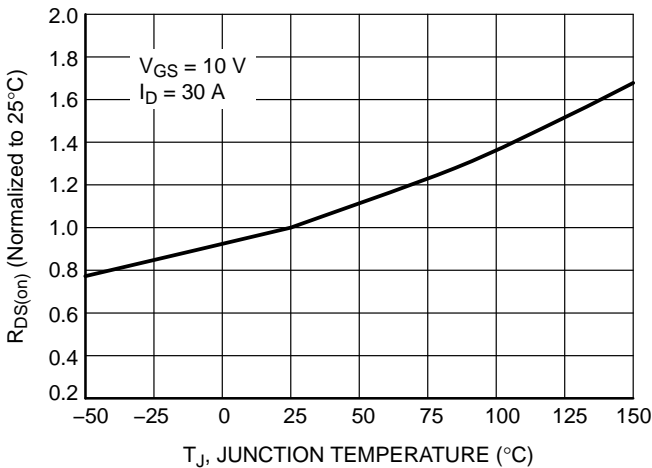


Figure 19. On-Resistance Variation with Temperature

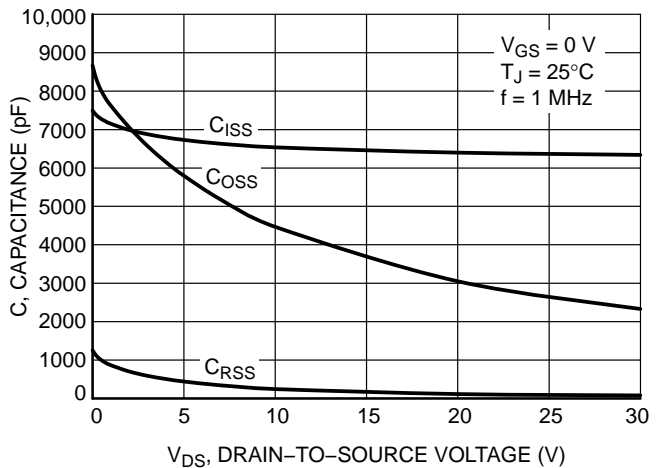


Figure 20. Capacitance Variation

NTMFD4C85N

TYPICAL CHARACTERISTICS – Q2

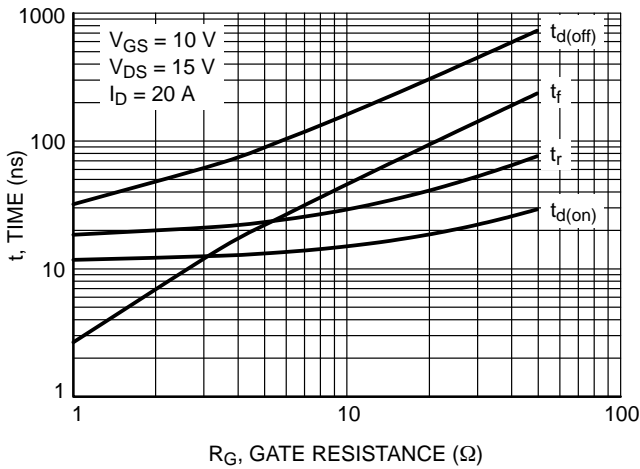


Figure 21. On-Region Characteristics

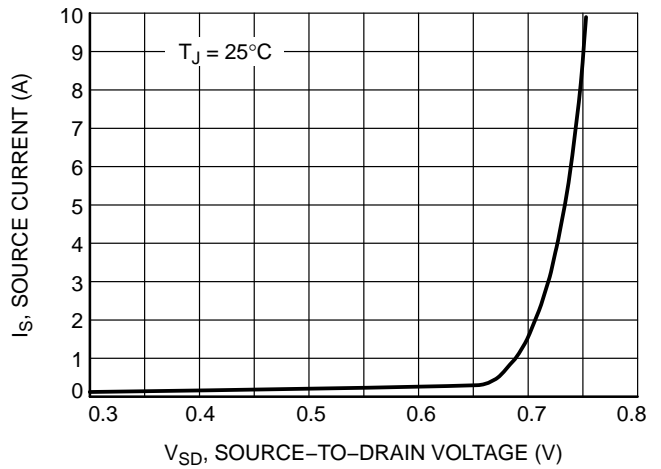


Figure 22. Diode Forward Voltage vs. Current

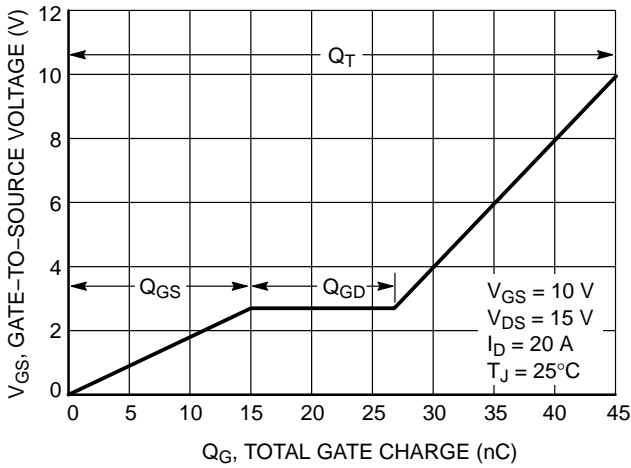


Figure 23. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

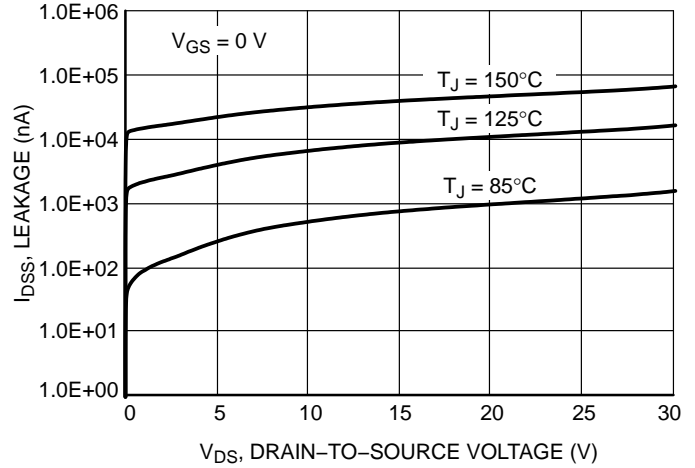


Figure 24. Drain-to-Source Leakage Current vs. Voltage

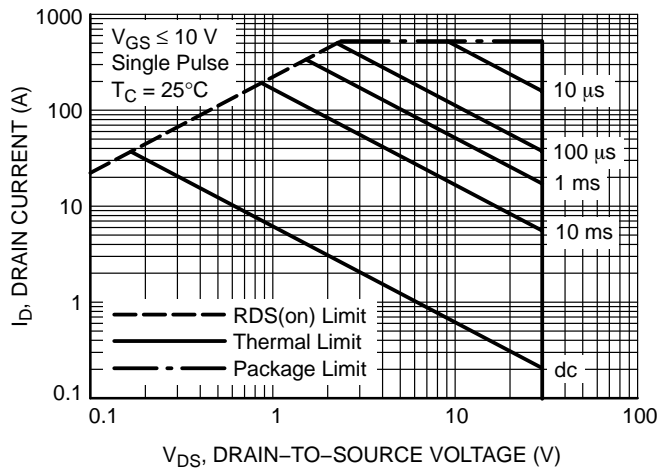


Figure 25. Maximum Rated Forward Biased Safe Operating Area

NTMFD4C85N

TYPICAL CHARACTERISTICS – Q2

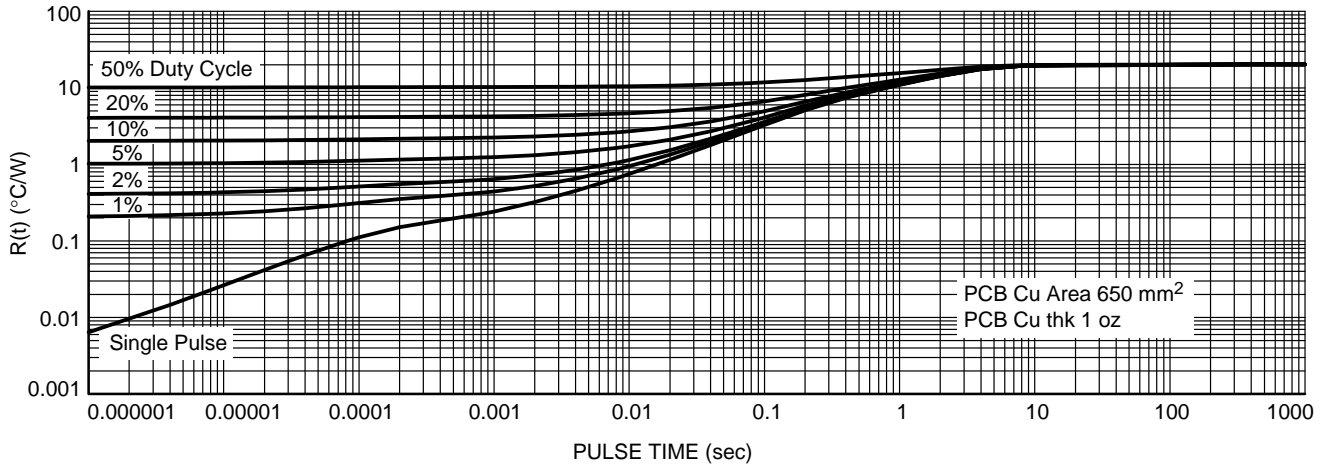


Figure 26. Thermal Characteristics

Ordering Information

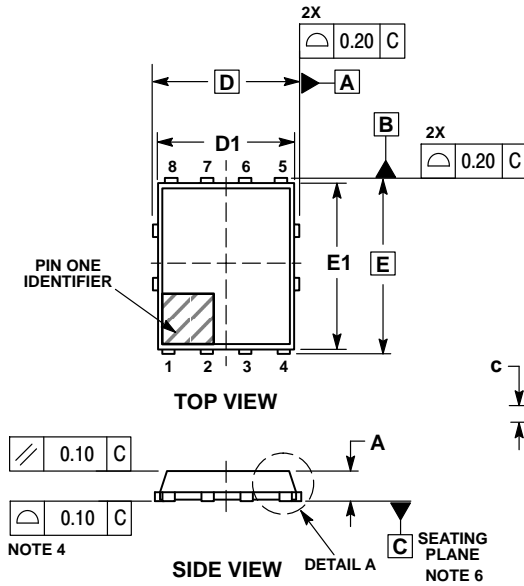
Device	Package	Shipping [†]
NTMFD4C85NT1G	DFN8 (Pb-Free)	1500 / Tape & Reel
NTMFD4C85NT3G	DFN8 (Pb-Free)	5000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTMFD4C85N

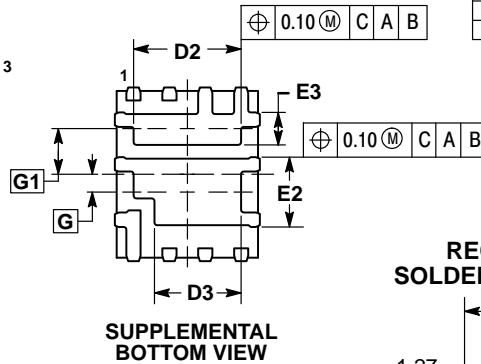
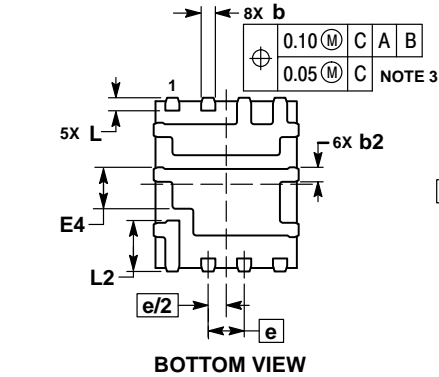
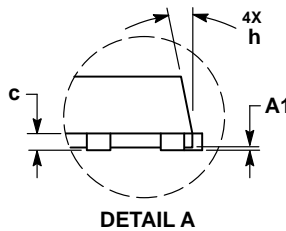
PACKAGE DIMENSIONS

DFN8 5x6, 1.27P PowerPhase FET
CASE 506CR
ISSUE B

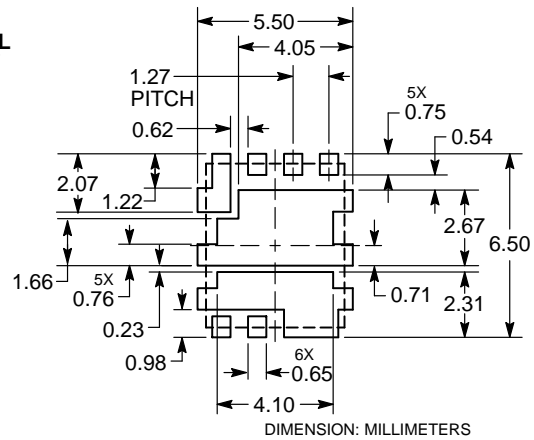


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSIONS b AND b1 APPLY TO PLATED TERMINAL AND ARE MEASURED BETWEEN 0.15 AND 0.25 MM FROM THE TIPS.
 4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
 5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
 6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

MILLIMETERS		
DIM	MIN	MAX
A	0.90	1.10
A1	0.00	0.05
b	0.40	0.60
b2	0.40	0.60
c	0.20	0.30
D	5.15 BSC	
D1	4.90	5.10
D2	3.70	3.90
D3	2.96	3.16
E	6.15 BSC	
E1	5.80	6.00
E2	2.37	2.57
E3	1.05	1.25
E4	1.36	1.56
e	1.27 BSC	
G	0.625 BSC	
G1	1.615 BSC	
h	12 °	
L	0.34	0.59
L2	1.68	1.93




RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTMFD4C85N

ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative